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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,673	03/17/2004	Jun Takasoh	403008	3315

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EXAMINER	
FILE, ERIN M	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,673	TAKASOH, JUN	
	Examiner	Art Unit	
	Erin M. File	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Friedman et al. (U.S. Pub. No. 2004/0114702) in view of Ono et al. (U.S. Pub. No. 2002/0097075) and Cai (U.S. Patent No. 6,396,360).

Claim 1, Friedman discloses:

- first-stage and second-stage latch circuits (fig. 5, first stage latches 5111 and 5112, second stages latches 551 and 552);
- additional first-stage and second-stage latch circuits (fig. 5, first stage latches 5111 and 5112, second stages latches 551 and 552);
- a selector circuit which receives an output of the first-stage latch circuit and an output of the additional first-stage latch circuit and outputs a re-timed signal in response (fig. 5, see selector at output of latches 5111 and 5112);
- a first exclusive OR circuit which receives an output of the second-stage latch circuit and an output of the additional second-stage latch circuit outputs a reference signal in response (fig. 5, XOR 541 receives input from second stages latches 551 and 552);

- wherein the voltage controlled oscillator is controlled by phase comparison polarity of the half-rate phase detector

Friedman fails to disclose:

- a latch delay circuit in a through-data path;
- a one-pulse delay circuit in the through-data path and receiving an output of the latch delay circuit and outputting through-data for generating a delay of one pulse
- a second exclusive OR circuit which receives the re-timed signal from the selector circuit and the through-data from the one-pulse delay circuit and outputs an output signal in response

However, Ono discloses:

- a latch delay circuit in a through-data path and a one-pulse delay circuit in the through-data path and receiving an output of the latch delay circuit and outputting through-data for generating a delay of one pulse (fig. 1, delay unit 22, the delay units in serial can be viewed as a single delay unit)
- a second exclusive OR circuit which receives the re-timed signal and the through-data from the delay circuit and outputs an output signal in response (fig. 1, logical operator 23)

Because Ono discloses his clock signal correction has the advantage of simple and accurate performance (abstract, lines 1-2). Because of this advantage it would be obvious to one skilled in the art to incorporate the logical operation as disclosed by Ono into the invention of Friedman. Although Friedman fails to disclose that the VCO is an N type LC VCO, Cai discloses a VCO which is is an N type LC VCO which he discloses

has the advantage of improved frequency stability and superior phase noise performance (col. 1, lines 36-38, col. 3, lines 26-30). Because of this advantage, it would have been obvious to one skilled in the art at the time of invention to incorporate the N type LC VCO as disclosed by Cai into the combined invention of Friedman and Ono.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: in claim 1 the recitation "a selector circuit which receives an output of the first-stage latch circuit and an output of the additional first-stage latch circuit and outputs a re-timed signal in response", it is unclear how or by what means a selection circuit is performing a retiming operation.

5. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: In Claim 1, "wherein the voltage controlled oscillator is an N type LC voltage controlled oscillator because of phase comparison polarity of the half-rate phase detector including the one-

pulse delay circuit", how the phase comparison polarity of the half rate detector is determined and how the VCO functions or is connected to the half rate phase detector is not properly described. Further in Claim 1, the inputs to the latch circuits are not defined or adequately described.

Allowable Subject Matter

6. Claims 2-7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is 5712726040. The examiner can normally be reached on M-F 1-9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 5712723024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Erin M. File

4/24/2007

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER